

L24 ANSWER 1 OF 13 USPATFULL on STN

AB A semiconductor light-emitting device has a semiconductor layer containing Al between a substrate and an active layer containing nitrogen, wherein Al and oxygen are removed from a growth chamber before growing said active layer and a concentration of oxygen incorporated into said active layer together with Al is set to a level such that said semiconductor light-emitting device can perform a continuous laser oscillation at room temperature.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:47628 USPATFULL

TI Semiconductor light-emitting device, surface-emission laser diode, and production apparatus thereof, production method, optical module and optical telecommunication system

IN Takahashi, Takashi, Miyagi, JAPAN  
Kaminishi, Morimasa, Miyagi, JAPAN  
Sato, Shunichi, Miyagi, JAPAN  
Itoh, Akihiro, Miyagi, JAPAN  
Jikutani, Naoto, Miyagi, JAPAN

PI US 2005040413 A1 20050224

AI US 2004-788086 A1 20040227 (10)

RLI Continuation-in-part of Ser. No. US 2002-105800, filed on 26 Mar 2002, GRANTED, Pat. No. US 6765232

PRAI JP 2001-89068 20010327

JP 2001-210462 20010711

JP 2001-253382 20010823

JP 2001-252537 20010823

JP 2001-262902 20010831

JP 2001-288367 20010921

JP 2001-292958 20010926

JP 2001-293353 20010926

JP 2001-297936 20010927

JP 2001-297937 20010927

JP 2001-297938 20010927

JP 2001-297939 20010927

JP 2001-390927 20011225

JP 2002-29822 20020206

JP 2002-65431 20020311

JP 2003-101620 20030404

JP 2003-77419 20030320

DT Utility

FS APPLICATION

LREP DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP, 2101 L Street, NW, Washington, DC, 20037

CLMN Number of Claims: 159

ECL Exemplary Claim: 1

DRWN 76 Drawing Page(s)

LN.CNT 10336

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 2 OF 13 USPATFULL on STN

AB In a method of manufacturing a silicon carbide substance, such as a film, a layer, a semiconductor, which is doped with an impurity, a carbonization process is executed after formation of a doped silicon substance which is obtained by carrying out a silicon deposition process and by a doping process of the impurity. Both the silicon deposition and the doping processes may be simultaneously or separately carried out prior to the carbonization process or may be continued during the carbonization process also. At any rate, the carbonization process is intermittently carried out. A unit process of composed of a combination of the silicon deposition process, the doping process, and the carbonization process may be repeated a plurality times, for example, 2000 times.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:334970 USPATFULL

TI Silicon carbide and method of manufacturing the same  
IN Nagasawa, Hiroyuki, Tokyo, JAPAN  
PA HOYA CORPORATION (non-U.S. corporation)  
PI US 2004266057 A1 20041230  
AI US 2004-890155 A1 20040714 (10)  
RLI Division of Ser. No. US 2001-924872, filed on 9 Aug 2001, ABANDONED  
PRAI JP 2000-242171 20000810  
DT Utility  
FS APPLICATION  
LREP SUGHRUE, MION, ZINN, MACPHEAK & SEAS, PLLC, 2100 Pennsylvania Avenue,  
N.W., Washington, DC, 20037-3213  
CLMN Number of Claims: 17  
ECL Exemplary Claim: 1  
DRWN 6 Drawing Page(s)  
LN.CNT 1187  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 3 OF 13 USPATFULL on STN

AB An (SiGe)C layer having a stoichiometric ratio of about 1:1 is locally formed on an Si layer, a large forbidden band width semiconductor device is prepared inside the layered structure thereof and an Si semiconductor integrated circuit is formed in the regions not formed with the layered structure, whereby high frequency high power operation of the device is enabled by the large forbidden band width semiconductor device and high performance is attained by hybridization of the Si integrated circuit.

AN 2004:324804 USPATFULL  
TI Semiconductor device, semiconductor circuit module and manufacturing method of the same  
IN Oda, Katsuya, Hachioji, JAPAN  
Sugii, Nobuyuki, Tokyo, JAPAN  
Miura, Makoto, Kokubunji, JAPAN  
Suzumura, Isao, Kokubunji, JAPAN  
Washio, Katsuyoshi, Tokorozawa, JAPAN  
PI US 2004256613 A1 20041223  
AI US 2004-790190 A1 20040302 (10)  
PRAI JP 2003-172912 20030618  
DT Utility  
FS APPLICATION  
LREP ANTONELLI, TERRY, STOUT & KRAUS, LLP, 1300 NORTH SEVENTEENTH STREET,  
SUITE 1800, ARLINGTON, VA, 22209-5889  
CLMN Number of Claims: 17  
ECL Exemplary Claim: 1  
DRWN 16 Drawing Page(s)  
LN.CNT 1955

L24 ANSWER 4 OF 13 USPATFULL on STN

AB A semiconductor light-emitting device has a semiconductor layer containing Al between a substrate and an active layer containing nitrogen, wherein Al and oxygen are removed from a growth chamber before growing said active layer and a concentration of oxygen incorporated into said active layer together with Al is set to a level such that said semiconductor light-emitting device can perform a continuous laser oscillation at room temperature.

AN 2004:304178 USPATFULL  
TI Semiconductor light-emitting device, surface-emission laser diode, and production apparatus thereof, production method, optical module and optical telecommunication system  
IN Takahashi, Takashi, Miyagi, JAPAN  
Kaminishi, Morimasa, Miyagi, JAPAN  
Sato, Shunichi, Miyagi, JAPAN  
Itoh, Akihiro, Miyagi, JAPAN  
Jikutani, Naoto, Kanagawa, JAPAN  
PI US 2004238832 A1 20041202  
AI US 2004-878282 A1 20040629 (10)  
RLI Division of Ser. No. US 2002-105800, filed on 26 Mar 2002, GRANTED, Pat. No. US 6765232

PRAI JP 2001-89068 20010327  
JP 2001-210462 20010711  
JP 2001-252537 20010823  
JP 2001-253382 20010823  
JP 2001-262902 20010831  
JP 2001-288367 20010921  
JP 2001-292958 20010926  
JP 2001-293353 20010926  
JP 2001-297936 20010927  
JP 2001-297937 20010927  
JP 2001-297938 20010927  
JP 2001-297939 20010927  
JP 2001-390927 20011225  
JP 2002-29822 20020206  
JP 2002-65431 20020311

DT Utility

FS APPLICATION

LREP DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP, 2101 L STREET NW, WASHINGTON,  
DC, 20037-1526

CLMN Number of Claims: 60

ECL Exemplary Claim: CLM-01-10

DRWN 71 Drawing Page(s)

LN.CNT 8023

L24 ANSWER 5 OF 13 USPATFULL on STN

AB A semiconductor light-emitting device has a semiconductor layer  
containing Al between a substrate and an active layer containing  
nitrogen, wherein Al and oxygen are removed from a growth chamber before  
growing said active layer and a concentration of oxygen incorporated  
into said active layer together with Al is set to a level such that said  
semiconductor light-emitting device can perform a continuous laser  
oscillation at room temperature.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:8756 USPATFULL

TI Semiconductor light-emitting device, surface-emission laser diode, and  
production apparatus thereof, production method, optical module and  
optical telecommunication system

IN Takahashi, Takashi, Miyagi, JAPAN  
Kaminishi, Morimasa, Miyagi, JAPAN  
Sato, Shunichi, Miyagi, JAPAN  
Itoh, Akihiro, Miyagi, JAPAN  
Jikutani, Naoto, Kanagawa, JAPAN

PI US 2003006429 A1 20030109

US 6765232 B2 20040720

AI US 2002-105800 A1 20020326 (10)

PRAI JP 2001-89068 20010327

JP 2001-210462 20010711

JP 2001-252537 20010823

JP 2001-253382 20010823

JP 2001-262902 20010831

JP 2001-288367 20010921

JP 2001-292958 20010926

JP 2001-293353 20010926

JP 2001-297936 20010927

JP 2001-297937 20010927

JP 2001-297938 20010927

JP 2001-297939 20010927

JP 2001-390927 20011225

JP 2002-29822 20020206

JP 2002-65431 20020311

DT Utility

FS APPLICATION

LREP DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP, 2101 L STREET NW, WASHINGTON,  
DC, 20037-1526

CLMN Number of Claims: 100

ECL Exemplary Claim: 2

DRWN 71 Drawing Page(s)

LN.CNT 8349

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 6 OF 13 USPATFULL on STN

AB A method for growing arrays of large-area device-size films of step-free (i.e., atomically flat) SiC surfaces for semiconductor electronic device applications is disclosed. This method utilizes a lateral growth process that better overcomes the effect of extended defects in the seed **crystal substrate** that limited the obtainable step-free area achievable by prior art processes. The step-free SiC surface is particularly suited for the heteroepitaxial growth of 3C (cubic) SiC, AlN, and GaN films used for the fabrication of both surface-sensitive devices (i.e., surface channel field effect transistors such as HEMT's and MOSFET's) as well as high-electric field devices (pn diodes and other solid-state power switching devices) that are sensitive to extended crystal defects.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:198741 USPATFULL

TI METHODS FOR **GROWTH** OF RELATIVELY LARGE STEP-FREE SIC **CRYSTAL** SURFACES

IN Neudeck, Philip G., Olmsted Falls, OH, UNITED STATES

Powell, J. Anthony, North Olmsted, OH, UNITED STATES

PI US 2002106842 A1 20020808

US 6461944 B2 20021008

AI US 2001-776998 A1 20010207 (9)

DT Utility

FS APPLICATION

LREP NASA GLENN RESEARCH CENTER, 21000 BROOKPARK ROAD, OFFICE OF CHIEF COUNSEL; MAIL STOP 500-118, CLEVELAND, OH, 44135

CLMN Number of Claims: 51

ECL Exemplary Claim: 1

DRWN 12 Drawing Page(s)

LN.CNT 1151

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 7 OF 13 USPATFULL on STN

AB A method utilizes sputter transport techniques to produce arrays or layers of self-forming, self-oriented columnar structures characterized as discrete, single-**crystal** Group III nitride posts or columns on various **substrates**. The columnar structure is formed in a single growth step, and therefore does not require processing steps for depositing, patterning, and etching growth masks. A Group III metal source vapor is produced by sputtering a target, for combination with nitrogen supplied from a nitrogen-containing source gas. The III/V ratio is adjusted or controlled to create a Group III metal-rich environment within the reaction chamber conducive to preferential column growth. The reactant vapor species are deposited on the **growth** surface to **produce** single-**crystal** M<sub>2</sub>sup.IIIIN columns thereon. The columns can be employed as a strain-relieving platform for the growth of continuous, low defect-density, bulk materials. Additionally, the growth conditions can be readjusted to effect columnar epitaxial overgrowth, wherein coalescence of the Group III nitride material occurs at the tops of the columns, thereby forming a substantially continuous layer upon which additional layers can be deposited. The intervening presence of the column structure mitigates thermal mismatch stress between substrates, films, or other layers above and below the columns. A high deposition rate sputter method utilizing a non-thermionic electron/plasma injector assembly is provided to carrying out one or more of the growth steps.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:154316 USPATFULL

TI Method and apparatus for producing M'''N columns and M'''N materials grown thereon

IN Cuomo, Jerome J., Cary, NC, UNITED STATES

Williams, N. Mark, Raleigh, NC, UNITED STATES

Hanser, Andrew David, Raleigh, NC, UNITED STATES

Carlson, Eric Porter, Raleigh, NC, UNITED STATES  
Thomas, Darin Taze, Raleigh, NC, UNITED STATES  
PI US 2002078881 A1 20020627  
US 6692568 B2 20040217  
AI US 2001-998024 A1 20011130 (9)  
PRAI US 2000-250297P 20001130 (60)  
US 2000-250337P 20001130 (60)  
DT Utility  
FS APPLICATION  
LREP JENKINS & WILSON, PA, 3100 TOWER BLVD, SUITE 1400, DURHAM, NC, 27707  
CLMN Number of Claims: 93  
ECL Exemplary Claim: 1  
DRWN 24 Drawing Page(s)  
LN.CNT 1929  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 8 OF 13 USPATFULL on STN

AB In a method of manufacturing a silicon carbide substance, such as a film, a layer, a semiconductor, which is doped with an impurity, a carbonization process is executed after formation of a doped silicon substance which is obtained by carrying out a silicon deposition process and by a doping process of the impurity. Both the silicon deposition and the doping processes may be simultaneously or separately carried out prior to the carbonization process or may be continued during the carbonization process also. At any rate, the carbonization process is intermittently carried out. A unit process of composed of a combination of the silicon deposition process, the doping process, and the carbonization process may be repeated a plurality times, for example, 2000 times.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:32296 USPATFULL  
TI Silicon carbide and method of manufacturing the same  
IN Nagasawa, Hiroyuki, Tokyo, JAPAN  
PA HOYA CORPORATION (non-U.S. corporation)  
PI US 2002019117 A1 20020214  
AI US 2001-924872 A1 20010809 (9)  
PRAI JP 2000-242171 20000810  
DT Utility  
FS APPLICATION  
LREP SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC, 2100 Pennsylvania Avenue, N.W., Washington, DC, 20037-3213  
CLMN Number of Claims: 19  
ECL Exemplary Claim: 1  
DRWN 6 Drawing Page(s)  
LN.CNT 1194  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 9 OF 13 USPATFULL on STN

AB To form a contact layer on source and drain electrodes of a stagger-type TFT, a conductive material is selectively stuck to the surface of the source and drain electrodes and a contact layer is selectively deposited by using the conductive material as growth species to form an active semiconductor layer on the contact layer. For an inverted-stagger-type TFT, a conductive material is selectively deposited on the surface of a contact layer to use the selectively deposited conductive material as source and drain electrodes so that patterning is unnecessary. To selectively deposit a contact layer of a TFT by alternately repeating etching and deposition, the temperature for the etching is set to 200° C. or lower. A contaminated layer on the surface of a semiconductor film serving as an active semiconductor layer and contact layer of a TFT is removed by plasma at the temperature of 200° C. or lower. For a stagger-type thin-film transistor, the hydrogen or halogen content of an insulating film serving as the substrate of source and drain electrodes is increased. For an inverted-stagger thin-film transistor, the hydrogen or halogen content of an insulating film serving as a channel protective film is increased. Thus, the etching rate of the surfaces of these insulating films by plasma increases.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 1999:30656 USPATFULL  
TI Method for fabricating thin-film transistor  
IN Yanai, Ken-ichi, Kawasaki, Japan  
Tanaka, Tsutomu, Kawasaki, Japan  
Ohgata, Koji, Kawasaki, Japan  
Takizawa, Yutaka, Kawasaki, Japan  
Oki, Ken-ichi, Kawasaki, Japan  
Hirano, Takuya, Kawasaki, Japan  
PA Fujitsu Limited, Kawasaki, Japan (non-U.S. corporation)  
PI US 5879973 19990309  
AI US 1995-510563 19950802 (8)  
RLI Division of Ser. No. US 1993-102248, filed on 5 Aug 1993, now patented,  
Pat. No. US 5470768  
PRAI JP 1992-211491 19920807  
JP 1992-212554 19920810  
JP 1992-232656 19920810  
JP 1993-181063 19930722  
DT Utility  
FS Granted  
EXNAM Primary Examiner: Trinh, Michael  
LREP Staas & Halsey  
CLMN Number of Claims: 7  
ECL Exemplary Claim: 1  
DRWN 84 Drawing Figure(s); 36 Drawing Page(s)  
LN.CNT 1770

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 10 OF 13 USPATFULL on STN

AB Oxide material, on a substrate, in a reactor, is etched by dissolving a hydrogen halide reaction product in a liquid phase reaction product. Both the hydrogen halide and liquid phase reaction products are produced through a chemical reaction of a reactive gas containing hydrogen and halogen elements as well as at least one gaseous compound which has been remotely activated. The liquid phase reaction product is obtained by condensation on the oxide material. The use of charged particle beams and irradiating light is discussed.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 91:54458 USPATFULL  
TI Method of oxide etching with condensed plasma reaction product  
IN Nishino, Hirotaka, Yokohama, Japan  
Hayasaka, Nobuo, Yokohama, Japan  
Okano, Haruo, Tokyo, Japan  
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)  
PI US 5030319 19910709  
AI US 1989-457946 19891227 (7)  
PRAI JP 1988-327594 19881227  
DT Utility  
FS Granted  
EXNAM Primary Examiner: Fisher, Richard V.; Assistant Examiner: Bruckner, John J.  
LREP Foley & Lardner  
CLMN Number of Claims: 6  
ECL Exemplary Claim: 1  
DRWN 36 Drawing Figure(s); 19 Drawing Page(s)  
LN.CNT 1576

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 11 OF 13 USPAT2 on STN

AB A semiconductor light-emitting device has a semiconductor layer containing Al between a substrate and an active layer containing nitrogen, wherein Al and oxygen are removed from a growth chamber before growing said active layer and a concentration of oxygen incorporated into said active layer together with Al is set to a level such that said semiconductor light-emitting device can perform a continuous laser oscillation at room temperature.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:8756 USPAT2  
TI Semiconductor light-emitting device, surface-emission laser diode, and  
production apparatus thereof, production method, optical module and  
optical telecommunication system  
IN Takahashi, Takashi, Miyagi, JAPAN  
Kaminishi, Morimasa, Miyagi, JAPAN  
Sato, Shunichi, Miyagi, JAPAN  
Itoh, Akihiro, Miyagi, JAPAN  
Jikutani, Naoto, Kanagawa, JAPAN  
PA Ricoh Company, Ltd., Tokyo, JAPAN (non-U.S. corporation)  
PI US 6765232 B2 20040720  
AI US 2002-105800 20020326 (10)  
PRAI JP 2001-89068 20010327  
JP 2001-210462 20010711  
JP 2001-252537 20010823  
JP 2001-253382 20010823  
JP 2001-262902 20010831  
JP 2001-288367 20010921  
JP 2001-292958 20010926  
JP 2001-293353 20010926  
JP 2001-297936 20010927  
JP 2001-297937 20010927  
JP 2001-297938 20010927  
JP 2001-297939 20010927  
JP 2001-390927 20011225  
JP 2002-29822 20020206  
JP 2002-65431 20020311  
DT Utility  
FS GRANTED  
EXNAM Primary Examiner: Nelms, David; Assistant Examiner: Tran, Mai-Huong  
LREP Dickstein Shapiro Morin & Oshinsky LLP  
CLMN Number of Claims: 44  
ECL Exemplary Claim: 1  
DRWN 115 Drawing Figure(s); 71 Drawing Page(s)  
LN.CNT 7800

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 12 OF 13 USPAT2 on STN

AB A method for growing arrays of large-area device-size films of step-free  
(i.e., atomically flat) SiC surfaces for semiconductor electronic device  
applications is disclosed. This method utilizes a lateral growth process  
that better overcomes the effect of extended defects in the seed  
**crystal substrate** that limited the obtainable  
step-free area achievable by prior art processes. The step-free SiC  
surface is particularly suited for the heteroepitaxial growth of 3C  
(cubic) SiC, AlN, and GaN films used for the fabrication of both  
surface-sensitive devices (i.e., surface channel field effect  
transistors such as HEMT's and MOSFET's) as well as high-electric field  
devices (pn diodes and other solid-state power switching devices) that  
are sensitive to extended crystal defects.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:198741 USPAT2  
TI Methods for **growth** of relatively large step-free SiC  
**crystal** surfaces  
IN Neudeck, Philip G., Olmsted Falls, OH, United States  
Powell, J. Anthony, North Olmsted, OH, United States  
PA The United States of America as represented by the Administrator of the  
National Aeronautics and Space Administration, Washington, DC, United  
States (U.S. government)  
PI US 6461944 B2 20021008  
AI US 2001-776998 20010207 (9)  
DT Utility  
FS GRANTED  
EXNAM Primary Examiner: Elms, Richard; Assistant Examiner: Luhrs, Michael K.  
LREP Stone, Kent N.

CLMN Number of Claims: 51  
ECL Exemplary Claim: 1  
DRWN 18 Drawing Figure(s); 12 Drawing Page(s)  
LN.CNT 1162  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L24 ANSWER 13 OF 13 USPAT2 on STN

AB A method utilizes sputter transport techniques to produce arrays or layers of self-forming, self-oriented columnar structures characterized as discrete, single-crystal Group III nitride posts or columns on various substrates. The columnar structure is formed in a single growth step, and therefore does not require processing steps for depositing, patterning, and etching growth masks. A Group III metal source vapor is produced by sputtering a target, for combination with nitrogen supplied from a nitrogen-containing source gas. The III/V ratio is adjusted or controlled to create a Group III metal-rich environment within the reaction chamber conducive to preferential column growth. The reactant vapor species are deposited on the growth surface to produce single-crystal M.sup.IIIIN columns thereon. The columns can be employed as a strain-relieving platform for the growth of continuous, low defect-density, bulk materials. Additionally, the growth conditions can be readjusted to effect columnar epitaxial overgrowth, wherein coalescence of the Group III nitride material occurs at the tops of the columns, thereby forming a substantially continuous layer upon which additional layers can be deposited. The intervening presence of the column structure mitigates thermal mismatch stress between substrates, films, or other layers above and below the columns. A high deposition rate sputter method utilizing a non-thermionic electron/plasma injector assembly is provided to carrying out one or more of the growth steps.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:154316 USPAT2  
TI Method and apparatus for producing MIIIN columns and MIIIN materials grown thereon  
IN Cuomo, Jerome J., Cary, NC, United States  
Williams, N. Mark, Raleigh, NC, United States  
Hanser, Andrew David, Raleigh, NC, United States  
Carlson, Eric Porter, Raleigh, NC, United States  
Thomas, Darin Taze, Raleigh, NC, United States  
PA Kyma Technologies, Inc., Raleigh, NC, United States (U.S. corporation)  
PI US 6692568 B2 20040217  
AI US 2001-998024 20011130 (9)  
PRAI US 2000-250297P 20001130 (60)  
US 2000-250337P 20001130 (60)  
DT Utility  
FS GRANTED  
EXNAM Primary Examiner: Hiteshew, Felisa Carla  
LREP Jenkins, Wilson & Taylor, P.A.  
CLMN Number of Claims: 93  
ECL Exemplary Claim: 1  
DRWN 37 Drawing Figure(s); 20 Drawing Page(s)  
LN.CNT 1930  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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(FILE 'HOME' ENTERED AT 08:30:29 ON 18 JUL 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 08:30:46 ON 18 JUL 2005

L1 400910 S (GROW? OR PRODUC? OR MANUFACTUR?) (8A) (CRYSTAL#)  
L2 142170 S (CRYSTAL#) (8A) (SUBSTRATE#)  
L3 69516 S (SUBLIMAT?)  
L4 52452 S (GAS? (6A) FLOW?) (8A) (CHAMBER#)  
L5 384 S (REACTIV? (6A) GAS?) (8A) (BOND?)  
L6 106 S (REACTIVE (8A) GAS?) (8A) (BUFFER? (6A) GAS?)



L7 6615160 S (INTERGRAT OR REACT?)  
L8 1372111 S (HE OR HELIUM OR AR OR ARGON)  
L9 22859 S (ETCH?) (8A) (H2 OR HYDROGEN)  
L10 189607 S (SILANE OR SILICON(W)TETRACHLORIDE OR TRIMETHYLSILANE)  
L11 55475 S (METHANE AND PROPANE)  
L12 0 S L1 AND L2 AND L3 AND L4 AND L5 AND L6  
L13 189 S (HEAT?) (8A) (BUFFER(W)GAS?)  
L14 88 S L1 AND L2 AND L3 AND L4  
L15 0 S L13 AND L14  
L16 30608 S (REACTOR(10A)WALL#)  
L17 12 S L14 AND L16  
L18 320 S (FLOW?(10A)BUFFER(W)GAS?)  
L19 0 S L14 AND L18  
L20 3838811 S (INHIBIT? OR STOP? OR ERRADICAT?)  
L21 33 S L14 AND L20  
L22 9102 S (BUFFER(W)GAS?)  
L23 0 S L21 AND L22  
L24 13 S BUFFER? AND L21

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Search History

STN

=> d 117 1-12 abs, bib

(HEADPLUS, WSPATALL, JAP210, INSPED)

7/18/05

L17 ANSWER 1 OF 12 USPATFULL on STN

AB Methods are provided for treating germanium surfaces in preparation for subsequent deposition, particularly gate dielectric deposition by atomic layer deposition (ALD). Prior to depositing, the germanium surface is treated with plasma products or thermally reacted with vapor reactants. Examples of surface treatments leave oxygen bridges, nitrogen bridges, --OH, --NH and/or --NH.sub.2 terminations that more readily adsorb ALD reactants. The surface treatments avoid deep penetration of the reactants into the germanium bulk but improve nucleation.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:124503 USPATFULL  
TI Surface preparation prior to deposition on germanium  
IN Wilk, Glen, Scottsdale, AZ, UNITED STATES  
PI US 2005106893 A1 20050519  
AI US 2004-910551 A1 20040803 (10)  
PRAI US 2003-492408P 20030804 (60)  
DT Utility  
FS APPLICATION  
LREP KNOBBE MARTENS OLSON & BEAR LLP, 2040 MAIN STREET, FOURTEENTH FLOOR,  
IRVINE, CA, 92614, US  
CLMN Number of Claims: 33  
ECL Exemplary Claim: 1  
DRWN 4 Drawing Page(s)  
LN.CNT 976

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 2 OF 12 USPATFULL on STN

AB A single-wafer, chemical vapor deposition reactor is provided with hydrogen and silicon source gas suitable for epitaxial silicon deposition, as well as a safe mixture of oxygen in a non-reactive gas. Methods are provided for forming oxide and silicon layers within the same chamber. In particular, a sacrificial oxidation is performed, followed by a hydrogen bake to sublime the oxide and leave a clean substrate. Epitaxial deposition can follow in situ. A protective oxide can also be formed over the epitaxial layer within the same chamber, preventing contamination of the critical epitaxial layer. Alternatively, the oxide layer can serve as the gate dielectric, and a polysilicon gate layer can be formed in situ over the oxide.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:264779 USPATFULL  
TI In situ growth of oxide and silicon layers  
IN Ferro, Armand, Phoenix, AZ, UNITED STATES  
Raaismakers, Ivo, Phoenix, AZ, UNITED STATES  
Foster, Derrick, Scottsdale, AZ, UNITED STATES  
PI US 2004206297 A1 20041021  
AI US 2004-841369 A1 20040506 (10)  
RLI Continuation of Ser. No. US 1999-227679, filed on 8 Jan 1999, GRANTED,  
Pat. No. US 6749687  
PRAI US 1998-70991P 19980109 (60)  
DT Utility  
FS APPLICATION  
LREP KNOBBE MARTENS OLSON & BEAR LLP, 2040 MAIN STREET, FOURTEENTH FLOOR,  
IRVINE, CA, 92614  
CLMN Number of Claims: 26  
ECL Exemplary Claim: 1  
DRWN 4 Drawing Page(s)  
LN.CNT 956

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 3 OF 12 USPATFULL on STN

AB Methods are provided herein for treating substrate surfaces in preparation for subsequent nucleation-sensitive depositions (e.g., polysilicon or poly-SiGe) and adsorption-driven deposition (e.g. atomic

layer deposition or ALD). Prior to depositing, the surface is treated with non-depositing plasma products. The treated surface more readily nucleates polysilicon and poly-SiGe (such as for a gate electrode), or more readily adsorbs ALD reactants (such as for a gate dielectric). The surface treatment provides surface moieties more readily susceptible to a subsequent deposition reaction, or more readily susceptible to further surface treatment prior to deposition. By changing the surface termination of the substrate with a low temperature radical treatment, subsequent deposition is advantageously facilitated without depositing a layer of any appreciable thickness and without significantly affecting the bulk properties of the underlying material. Preferably less than 10 Å of the bulk material incorporates the excited species, which can include fluorine, chlorine and particularly nitrogen excited species.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:190331 USPATFULL  
TI Surface preparation prior to deposition  
IN Pomarede, Christophe F., Phoenix, AZ, UNITED STATES  
Roberts, Jeff, Chandler, AZ, UNITED STATES  
Shero, Eric J., Phoenix, AZ, UNITED STATES  
PI US 2004147101 A1 20040729  
AI US 2003-626217 A1 20030724 (10)  
RLI Division of Ser. No. US 2001-944734, filed on 31 Aug 2001, GRANTED, Pat.  
No. US 6613695  
PRAI US 2000-253693P 20001124 (60)  
US 2001-283584P 20010413 (60)  
DT Utility  
FS APPLICATION  
LREP KNOBBE MARTENS OLSON & BEAR LLP, 2040 MAIN STREET, FOURTEENTH FLOOR,  
IRVINE, CA, 92614  
CLMN Number of Claims: 15  
ECL Exemplary Claim: 1  
DRWN 5 Drawing Page(s)  
LN.CNT 1079

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 4 OF 12 USPATFULL on STM

AB Methods are provided herein for treating substrate surfaces in preparation for subsequent nucleation-sensitive depositions (e.g., polysilicon or poly-SiGe) and adsorption-driven deposition (e.g. atomic layer deposition or ALD). Prior to depositing, the surface is treated with non-depositing plasma products. The treated surface more readily nucleates polysilicon and poly-SiGe (such as for a gate electrode), or more readily adsorbs ALD reactants (such as for a gate dielectric). The surface treatment provides surface moieties more readily susceptible to a subsequent deposition reaction, or more readily susceptible to further surface treatment prior to deposition. By changing the surface termination of the substrate with a low temperature radical treatment, subsequent deposition is advantageously facilitated without depositing a layer of any appreciable thickness and without significantly affecting the bulk properties of the underlying material. Preferably less than 10 Å of the bulk material incorporates the excited species, which can include fluorine, chlorine and particularly nitrogen excited species.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:158818 USPATFULL  
TI Surface preparation prior to deposition  
IN Pomarede, Christophe F., Phoenix, AZ, UNITED STATES  
Roberts, Jeff, Chandler, AZ, UNITED STATES  
Shero, Eric J., Phoenix, AZ, UNITED STATES  
PI US 2004121620 A1 20040624  
AI US 2003-626212 A1 20030724 (10)  
RLI Continuation of Ser. No. US 2001-944734, filed on 31 Aug 2001, GRANTED,  
Pat. No. US 6613695  
PRAI US 2000-253693P 20001124 (60)  
US 2001-283584P 20010413 (60)  
DT Utility  
FS APPLICATION

LREP KNOBBE MARTENS OLSON & BEAR LLP, 2040 MAIN STREET, FOURTEENTH FLOOR,  
IRVINE, CA, 92614  
CLMN Number of Claims: 19  
ECL Exemplary Claim: 1  
DRWN 5 Drawing Page(s)  
LN.CNT 1086  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 5 OF 12 USPATFULL on STN

AB A single-wafer, chemical vapor deposition reactor is provided with hydrogen and silicon source gas suitable for epitaxial silicon deposition, as well as a safe mixture of oxygen in a non-reactive gas. Methods are provided for forming oxide and silicon layers within the same chamber. In particular, a sacrificial oxidation is performed, followed by a hydrogen bake to sublime the oxide and leave a clean substrate. Epitaxial deposition can follow in situ. A protective oxide can also be formed over the epitaxial layer within the same chamber, preventing contamination of the critical epitaxial layer. Alternatively, the oxide layer can serve as the gate dielectric, and a polysilicon gate layer can be formed in situ over the oxide.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:146817 USPATFULL  
TI In situ growth of oxide and silicon layers  
IN Ferro, Armand, Phoenix, AZ, United States  
Raaismakers, Ivo, Phoenix, AZ, United States  
Foster, Derrick, Scottsdale, AZ, United States  
PA ASM America, Inc., Phoenix, AZ, United States (U.S. corporation)

PI US 6749687 B1 20040615  
AI US 1999-227679 19990108 (9)  
PRAI US 1998-70991P 19980109 (60)

DT Utility

FS GRANTED

EXNAM Primary Examiner: Norton, Nadine G.; Assistant Examiner: Anderson, Matthew A.

LREP Knobbe, Martens, Olson & Bear, LLP

CLMN Number of Claims: 15

ECL Exemplary Claim: 1

DRWN 5 Drawing Figure(s); 4 Drawing Page(s)

LN.CNT 948

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 6 OF 12 USPATFULL on STN

AB A single-wafer, chemical vapor deposition reactor is provided with hydrogen and silicon source gas suitable for epitaxial silicon deposition, as well as a safe mixture of oxygen in a non-reactive gas. Methods are provided for forming oxide and silicon layers within the same chamber. In particular, a sacrificial oxidation is performed, followed by a hydrogen bake to sublime the oxide and leave a clean substrate. Epitaxial deposition can follow in situ. A protective oxide can also be formed over the epitaxial layer within the same chamber, preventing contamination of the critical epitaxial layer. Alternatively, the oxide layer can serve as the gate dielectric, and a polysilicon gate layer can be formed in situ over the oxide.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:106382 USPATFULL

TI In situ growth of oxide and silicon layers

IN Ferro, Armand, Phoenix, AZ, UNITED STATES  
Raaismakers, Ivo, Phoenix, AZ, UNITED STATES  
Foster, Derrick, Scottsdale, AZ, UNITED STATES

PI US 2003073293 A1 20030417

AI US 2002-293795 A1 20021112 (10)

RLI Continuation of Ser. No. US 1999-227679, filed on 8 Jan 1999, PENDING

PRAI US 1998-70991P 19980109 (60)

DT Utility

FS APPLICATION

LREP KNOBBE MARTENS OLSON & BEAR LLP, 2040 MAIN STREET, FOURTEENTH FLOOR,

IRVINE, CA, 92614  
CLMN Number of Claims: 32  
ECL Exemplary Claim: 1  
DRWN 4 Drawing Page(s)  
LN.CNT 944

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 7 OF 12 USPATFULL on STN

AB A high k dielectric film and methods for forming the same are disclosed. The high k material includes two peaks of impurity concentration, particularly nitrogen, such as at a lower interface and upper interface, making the layer particularly suitable for transistor gate dielectric applications. The methods of formation include low temperature processes, particularly CVD using a remote plasma generator and atomic layer deposition using selective incorporation of nitrogen in the cyclic process. Advantageously, nitrogen levels are tailored during the deposition process and temperatures are low enough to avoid interdiffusion and allow maintenance of the desired impurity profile.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:106064 USPATFULL  
TI Incorporation of nitrogen into high k dielectric film  
IN Shero, Eric J., Phoenix, AZ, UNITED STATES  
Pomarede, Christophe, UNITED STATES  
PI US 2003072975 A1 20030417  
AI US 2002-260370 A1 20020926 (10)  
PRAI US 2001-326830P 20011002 (60)  
DT Utility  
FS APPLICATION  
LREP KNOBBE MARTENS OLSON & BEAR LLP, 2040 MAIN STREET, FOURTEENTH FLOOR,  
IRVINE, CA, 92614  
CLMN Number of Claims: 23  
ECL Exemplary Claim: 1  
DRWN 10 Drawing Page(s)  
LN.CNT 1394

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 8 OF 12 USPATFULL on STN

AB Abstract of Disclosure

Methods are provided herein for forming electrode layers over high dielectric constant (high k) materials. In the illustrated embodiments, a high k gate dielectric, such as zirconium oxide, is protected from reduction during a subsequent deposition of silicon-containing gate electrode. In particular, a seed deposition phase includes conditions designed for minimizing hydrogen reduction of the gate dielectric, including low hydrogen content, low temperatures and/or low partial pressures of the silicon source gas. Conditions are preferably changed for higher deposition rates and deposition continues in a bulk phase. Desirably, though, hydrogen diffusion is still minimized by controlling the above-noted parameters. In one embodiment, high k dielectric reduction is minimized through omission of a hydrogen carrier gas. In another embodiment, higher order silanes aid in reducing hydrogen content for a given deposition rate.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:308005 USPATFULL  
TI Integration of High K Gate Dielectric  
IN Pomarede, Christophe F., 3328 E. Glenhaven Drive, Phoenix, AZ, UNITED STATES 85048  
Givens, Michael E., 3527 E. Sahuaro Drive, Phoenix, AZ, UNITED STATES 85028  
Shero, Eric J., 5702 E. Piedmont #2293, Phoenix, AZ, UNITED STATES 85044  
Todd, Michael A., 7041 N. 14th Place, Phoenix, AZ, UNITED STATES 85020  
PI US 2002173130 A1 20021121  
AI US 2002-74722 A1 20020211 (10)

PRAI US 2001-60268337 20010212  
US 2001-60279256 20010327  
US 2001-60332696 20011113  
DT Utility  
FS APPLICATION  
LREP Knobbe, Martens,, Olson & Bear, LLP, 620 Newport Center Drive ,  
Sixteenth Floor, Newport Beach, CA, 92660  
CLMN Number of Claims: 39  
ECL Exemplary Claim: 1  
DRWN 9 Drawing Page(s)  
LN.CNT 1122  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 9 OF 12 USPATFULL on STN  
AB Methods are provided herein for treating substrate surfaces in preparation for subsequent nucleation-sensitive depositions (e.g., polysilicon or poly-SiGe) and adsorption-driven deposition (e.g. atomic layer deposition or ALD). Prior to depositing, the surface is treated with non-depositing plasma products. The treated surface more readily nucleates polysilicon and poly-SiGe (such as for a gate electrode), or more readily adsorbs ALD reactants (such as for a gate dielectric). The surface treatment provides surface moieties more readily susceptible to a subsequent deposition reaction, or more readily susceptible to further surface treatment prior to deposition. By changing the surface termination of the substrate with a low temperature radical treatment, subsequent deposition is advantageously facilitated without depositing a layer of any appreciable thickness and without significantly affecting the bulk properties of the underlying material. Preferably less than 10 Å of the bulk material incorporates the excited species, which can include fluorine, chlorine and particularly nitrogen excited species.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:185714 USPATFULL  
TI Surface preparation prior to deposition  
IN Pomarede, Christophe F., Phoenix, AZ, UNITED STATES  
Roberts, Jeff, Chandler, AZ, UNITED STATES  
Shero, Eric J., Phoenix, AZ, UNITED STATES  
PI US 2002098627 A1 20020725  
US 6613695 B2 20030902  
AI US 2001-944734 A1 20010831 (9)  
PRAI US 2000-253693P 20001124 (60)  
US 2001-283584P 20010413 (60)  
DT Utility  
FS APPLICATION  
LREP KNOBBE MARTENS OLSON & BEAR LLP, 620 NEWPORT CENTER DRIVE, SIXTEENTH  
FLOOR, NEWPORT BEACH, CA, 92660  
CLMN Number of Claims: 24  
ECL Exemplary Claim: 1  
DRWN 5 Drawing Page(s)  
LN.CNT 1106  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 10 OF 12 USPATFULL on STN  
AB A method of controlling the amount of impurity incorporation in a **crystal grown** by a chemical vapor deposition process. Conducted in a growth chamber, the method includes the controlling of the concentration of the **crystal growing** components in the **growth** chamber to affect the demand of particular **growth** sites within the **growing crystal** thereby controlling impurity incorporation into the **growth** sites.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 1998:6671 USPATFULL  
TI Compound semi-conductors and controlled doping thereof  
IN Larkin, David J., Valley City, OH, United States  
Neudeck, Philip G., Cleveland, OH, United States  
Powell, J. Anthony, North Olmsted, OH, United States

Matus, Lawrence G., Amherst, OH, United States  
PA Ohio Aerospace Institute, Brook Park, OH, United States (U.S. corporation)  
PI US 5709745 19980120  
AI US 1995-554201 19951106 (8)  
RLI Continuation-in-part of Ser. No. US 1994-276599, filed on 18 Jul 1994, now patented, Pat. No. US 5463978, issued on 7 Nov 1995 which is a continuation of Ser. No. US 1993-8650, filed on 25 Jan 1993, now abandoned  
DT Utility  
FS Granted  
EXNAM Primary Examiner: Garrett, Felisa  
LREP Vickers, Daniels & Young  
CLMN Number of Claims: 52  
ECL Exemplary Claim: 1  
DRWN 12 Drawing Figure(s); 6 Drawing Page(s)  
LN.CNT 2690  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 11 OF 12 USPATFULL on STN

AB Oxide material, on a substrate, in a reactor, is etched by dissolving a hydrogen halide reaction product in a liquid phase reaction product. Both the hydrogen halide and liquid phase reaction products are produced through a chemical reaction of a reactive gas containing hydrogen and halogen elements as well as at least one gaseous compound which has been remotely activated. The liquid phase reaction product is obtained by condensation on the oxide material. The use of charged particle beams and irradiating light is discussed.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 91:54458 USPATFULL  
TI Method of oxide etching with condensed plasma reaction product  
IN Nishino, Hirotaka, Yokohama, Japan  
Hayasaka, Nobuo, Yokohama, Japan  
Okano, Haruo, Tokyo, Japan  
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)  
PI US 5030319 19910709  
AI US 1989-457946 19891227 (7)  
PRAI JP 1988-327594 19881227  
DT Utility  
FS Granted  
EXNAM Primary Examiner: Fisher, Richard V.; Assistant Examiner: Bruckner, John J.  
LREP Foley & Lardner  
CLMN Number of Claims: 6  
ECL Exemplary Claim: 1  
DRWN 36 Drawing Figure(s); 19 Drawing Page(s)  
LN.CNT 1576  
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L17 ANSWER 12 OF 12 USPAT2 on STN

AB Methods are provided herein for treating substrate surfaces in preparation for subsequent nucleation-sensitive depositions (e.g., polysilicon or poly-SiGe) and adsorption-driven deposition (e.g. atomic layer deposition or ALD). Prior to depositing, the surface is treated with non-depositing plasma products. The treated surface more readily nucleates polysilicon and poly-SiGe (such as for a gate electrode), or more readily adsorbs ALD reactants (such as for a gate dielectric). The surface treatment provides surface moieties more readily susceptible to a subsequent deposition reaction, or more readily susceptible to further surface treatment prior to deposition. By changing the surface termination of the substrate with a low temperature radical treatment, subsequent deposition is advantageously facilitated without depositing a layer of any appreciable thickness and without significantly affecting the bulk properties of the underlying material. Preferably less than 10 Å of the bulk material incorporates the excited species, which can include fluorine, chlorine and particularly nitrogen excited species.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:185714 USPAT2

TI Surface preparation prior to deposition

IN Pomarede, Christophe F. Phoenix, AZ, United States

Roberts, Jeff, Chandler, AZ, United States

Shero, Eric J., Phoenix, AZ, United States

PA ASM America, Inc., Phoenix, AZ, United States (U.S. corporation)

PI US 6613695 B2 20030902

AI US 2001-944734 20010831 (9)

PRAI US 2000-253693P 20001124 (60)

US 2001-283584P 20010413 (60)

DT Utility

FS GRANTED

EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Lee, Hsien-Ming

LREP Knobbe, Martens, Olson & Bear LLP.

CLMN Number of Claims: 19

ECL Exemplary Claim: 1

DRWN 6 Drawing Figure(s); 5 Drawing Page(s)

LN.CNT 1086

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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(FILE 'HOME' ENTERED AT 08:30:29 ON 18 JUL 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 08:30:46 ON  
18 JUL 2005

L1 400910 S (GROW? OR PRODUC? OR MANUFACTUR?) (8A) (CRYSTAL#)  
L2 142170 S (CRYSTAL#) (8A) (SUBSTRATE#)  
L3 69516 S (SUBLIMAT?)  
L4 52452 S (GAS? (6A) FLOW?) (8A) (CHAMBER#)  
L5 384 S (REACTIV? (6A) GAS?) (8A) (BOND?)  
L6 106 S (REACTIVE (8A) GAS?) (8A) (BUFFER? (6A) GAS?)  
L7 6615160 S (INTERGRAT OR REACT?)  
L8 1372111 S (HE OR HELIUM OR AR OR ARGON)  
L9 22859 S (ETCH?) (8A) (H2 OR HYDROGEN)  
L10 189607 S (SILANE OR SILICON (W) TETRACHLORIDE OR TRIMETHYLSILANE)  
L11 55475 S (METHANE AND PROPANE)  
L12 0 S L1 AND L2 AND L3 AND L4 AND L5 AND L6  
L13 189 S (HEAT?) (8A) (BUFFER (W) GAS?)  
L14 88 S L1 AND L2 AND L3 AND L4  
L15 0 S L13 AND L14  
L16 30608 S (REACTOR (10A) WALL#)  
L17 12 S L14 AND L16

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